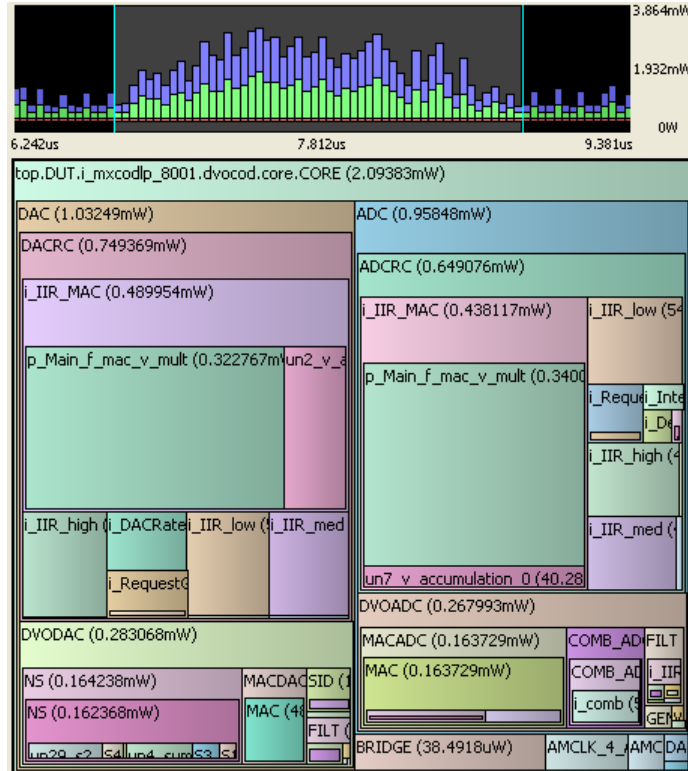


Power Consumption of logic parts of a SoC is one face of the coin, the other face of which is Noise Resilience of analog parts. Reducing the peaks of a dynamic mixed-signal power consumption simulation grants the consistent benefit of smoothing-out the disturbances threatening high-resolution analog parts, including sensitive read-margins of logic parts. Power analysis is best performed in the time domain, while noise resilience is best analyzed over the spectral domain.

SCROOGE 2.0 unifies hierarchical mixed-signal power consumption and provides the missing simulation capability!

KEY ENHANCEMENTS

- ✓ Unified hierarchical mixed-signal power consumption simulation
- ✓ Analog power consumption reporting
- ✓ Signal driven power simulation with testbench enable/disable
- ✓ Clock based leakage and dynamic cycle power consumption simulation
- ✓ Hierarchical browsing of power map, both online and as post-processing
- ✓ Extraction of cycle power signature: min, max, average and std deviation
- ✓ Streamlined graphic user interface
- ✓ Enhanced power consumption report with color scales
- ✓ Extended support of SPEF back-annotation
- ✓ Increased capacity and reduced SDF annotation memory requirements



DESCRIPTION OF THE ENHANCEMENTS

Optimizing the power consumption of a SoC requires being able to hierarchically simulate mixed-signal power at various accuracy levels, from time-accurate, through cycle-accurate, up to mode-accurate (from a Virtual Component point-of-view) and state-accurate (from a testbench point-of-view), thereby providing the means to efficiently assess and implement power saving techniques.

Clock-based power analysis enables cycle-accurate simulation by averaging the consumption over the clock period, providing analog, logic (leakage, internal and switching) and total power, and generating power consumption reports. Selection of a range of clock periods provides an intuitive hierarchical map view of the corresponding consumption.

Signal-enabled power analysis enables mode or state-based simulation by controlling the activation of power calculations during the transient analysis. A reset, simple enable, or complex expression associated to a controlling signal enables focusing the power display and reporting on a specific mode or state.



SCROOGE is available identically under Linux, Solaris and Windows.

Power consumption summary

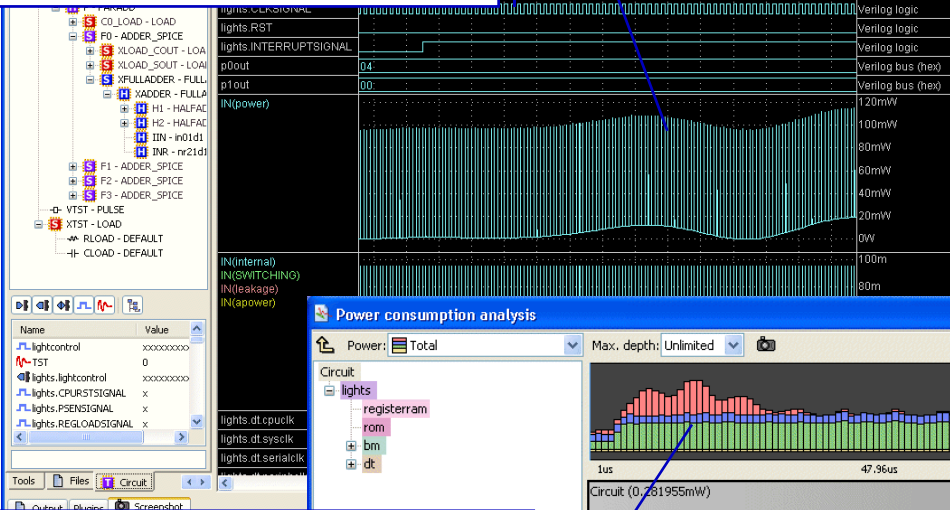
Transient power analysis summary

Transient analysis duration: 131.00846s

Design: lights
Including Clock-Tree emission

Design Top-level	Leakage	Internal	Switching	Analog	Total
Energy	1.1169kJ	20.775kJ	6.5036kJ	8.774kJ	37.17kJ
Power	8.5257uW	158.58uW	49.642uW	66.978uW	283.73uW
Percentage	3.00 %	55.89 %	17.50 %	23.61 %	100.00 %

Unified mixed power consumption representation



Cycle power representation

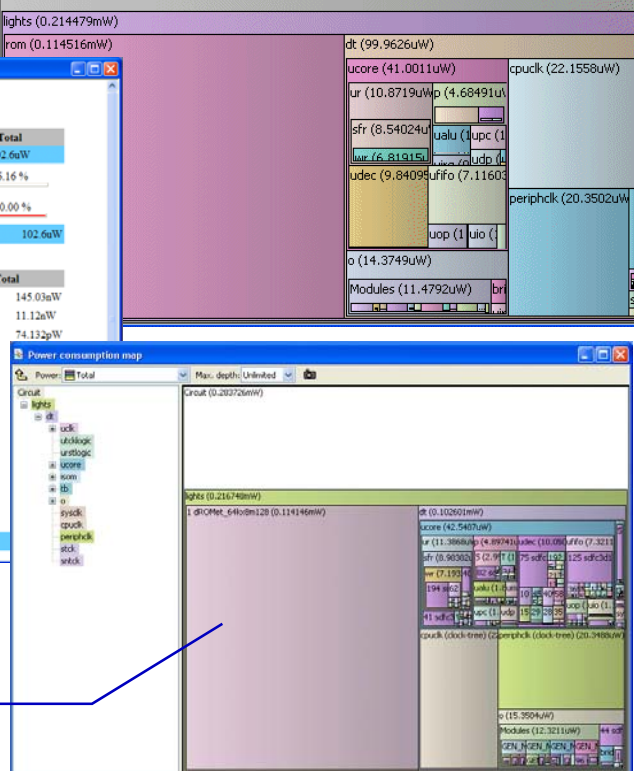
dt mean power from 0s to 131.25us

dt	Leakage	Internal	Switching	Analog	Total
Power	4.5257uW	48.48uW	49.596uW	0W	102.6uW
Percentage (absolute)	1.60 %	17.09 %	17.48 %	0.00 %	36.16 %
Percentage (relative)	4.41 %	47.25 %	48.34 %	0.00 %	100.00 %
dt	4.5257uW	48.48uW	49.596uW	0W	102.6uW

Sub-Cells	Leakage	Internal	Switching	Analog	Total
dt.ucik	3.3359uW	80.88uW	60.819uW	0W	145.03uW
dt.uscklogie	911.69pW	6.0962uW	4.1123uW	0W	11.12uW
dt.i_002_3	74.132pW	0W	0W	0W	74.132pW
dt.uscklogie	13.02uW	112.37uW	49.208uW	0W	174.6uW
dt.uscore	2.862uW	31.708uW	7.9787uW	0W	42.55uW
dt.tiom	21.572uW	107.98uW	182.75uW	0W	312.3uW
dt.tb	112.52uW	1.1753uW	6.4856uW	0W	120.18uW
dt.o	1.4926uW	13.456uW	401.95uW	0W	416.91uW
dt.sysck	284.4pW	26.026uW	233.15uW	0W	261.48uW
dt.cpuck	9.102uW	947.56uW	21.198uW	0W	977.86uW
dt.periphck	8.2485uW	859.52uW	19.481uW	0W	887.26uW
dt.stck	1.7064uW	0W	0W	0W	1.7064uW
dt.usck	284.4pW	0W	0W	0W	284.4pW
dt	4.5257uW	48.48uW	49.596uW	0W	102.6uW

Interactive power summary

Power map representation



MEDAL Presentation Sheet